

REPORT DOCUMENTATION PAGE

AFRL-SR-BL-TR-00-

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1. AGENCY USE ONLY (Leave blank)		2. REPORT DATE 12/23/98	3. REPORT TYPE AND DATES COVERED FINAL 10/1/94-9/30/98	
4. TITLE AND SUBTITLE ADVANCED SILICON FET PHYSICS AND DEVICE STRUCTURES			5. FUNDING NUMBERS F49620-94-1-0464	
6. AUTHOR(S) Prof. Chenming Hu Prof. Jeffrey Bokor				
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) UNIVERSITY OF CALIFORNIA Department of Electrical Engineering & Computer Sciences Berkeley, CA 94720			8. PERFORMING ORGANIZATION REPORT NUMBER	
9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES) Sponsoring Agency: Monitoring Agency: AFOSR, Bolling AFB DC 20332-0001 Program Manager: Dr. Gerald L. Witt, AFOSR/NE			10. SPONSORING / MONITORING AGENCY REPORT NUMBER	
11. SUPPLEMENTARY NOTES				
a. DISTRIBUTION / AVAILABILITY STATEMENT Approved for public release, distribution unlimited.			12. DISTRIBUTION CODE	
13. ABSTRACT (Maximum 200 words) The objectives of the project were to develop experimental techniques for characterizing the transport and hot carrier phenomena in advanced MOSFETs, to investigate the limits of gate oxide scaling, to develop engineering models for the relevant physical effects, and to incorporate the results in device simulators and in MOSFET models for circuit simulations. All the objectives have been met.				
14. SUBJECT TERMS MOSFET, hot carriers, gate oxide, circuit simulation			15. NUMBER OF PAGES 5	
			16. PRICE CODE	
17. SECURITY CLASSIFICATION OF REPORT UNCLASSIFIED	18. SECURITY CLASSIFICATION OF THIS PAGE UNCLASSIFIED	19. SECURITY CLASSIFICATION OF ABSTRACT UNCLASSIFIED	20. LIMITATION OF ABSTRACT	

20000120 096

Final Technical Report

Advanced Silicon FET Physics and Device Structures

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Grant Number:

F49620-94-1-0464

Reporting Period:

10/1/94 - 9/30/98

Final Technical Report F49620-94-1-0464

1. OVERVIEW

The objectives of the project were to develop experimental techniques for characterizing the transport and hot carrier phenomena in advanced MOSFETs, to investigate the limits of gate oxide scaling, to develop engineering models for the relevant physical effects, and to incorporate the results in device simulators and in MOSFET models for circuit simulations. All the objectives have been met.

A new experimental technique for studying hot carrier phenomena in semiconductors subjected to high electric fields was successfully developed. The method involves the generation of a high field strength terahertz (THz) electromagnetic pulse using femtosecond laser electro-optical techniques. This pulse is focused in a doped semiconductor sample and the transmitted and reflected fields are characterized. Carriers in the semiconductor are accelerated by the incident electric field pulse and if the field is sufficiently strong, the carrier distribution is significantly heated. In this event, the sample exhibits a nonlinear response to the applied field, which is clearly manifested in the transmitted and reflected fields. In order to successfully implement this method, new methods for generating strong THz fields were developed. The propagation of ultrashort THz pulses was carefully studied including the temporal and spatial details of the field distribution produced at the focus in the sample. Sensitive electro-optic detection techniques were also developed for use in these characterization studies as well as for the actual semiconductor experiments. What we observed in the experiments is a change in the shape of the THz absorption spectrum of n-doped GaAs as the THz field strength is increased. The effect is strongest at frequencies above 1 THz. Extensive simulations of the experiment were carried out, and there is at least a qualitative agreement between the simulations and the observations.

Using electrical measurements and advanced MOSFET technologies, we have studied the electron and hole mobilities in inversion layers over a wide range of oxide thicknesses and substrate doping concentrations including those expected for MOSFETs with 0.1 μ m and shorter channel lengths. We developed a model to predict the carrier mobilities for any given oxide thickness, threshold voltage and gate voltage. This directly challenges the conventional wisdom that holds that inversion layer mobilities are quite variable and unpredictable. This mobility model is used in a new model for circuit simulation, BSIM3v3, which has found instant success with the IC industry. It has been chosen by Sematech as the first industry standard model for circuit simulation and selected as an R&D 100 Award winner. The model has been transferred to hundreds of semiconductor companies. Other research results have also been incorporated into BSIM3 as described below. Some day, almost all the IC's in the world may be designed using this MOSFET model.

The velocity overshoot phenomenon in the inversion layer was studied by using the thick-gate uniform channel field MOS transistor. Using devices with sub-100nm channel lengths, we performed an extensive investigation of ballistic transport in inversion layer under uniform field condition. We experimentally studied the effects of a wide range of

parameters on the high-field transport of inversion layer electrons and holes. Our findings pointed to significant electron velocity overshoot at room temperature, dependence of the high-field drift velocity and velocity overshoot on the effective vertical field, and relative insensitivity of electron and hole mobility and velocity overshoot to moderate surface roughness. Our results were the most direct, comprehensive, and quantitative to date. The new quantitative data were used to calibrate a commercial device simulator, MEDICI. The calibrated simulator was further used to predict the impact of velocity overshoot on future MOSFETs. 20% current improvements are predicted for 0.1 μ m MOSFETs. An analytical model of MOSFET IV characteristics including velocity overshoot has been developed and may be incorporated in future BSIM MOSFET models.

We proposed that the impact of inversion layer quantization on MOSFET characteristics can be represented by an effective thickness of the inversion charge layer and that the layer thickness is a unique function of V_g , V_t , and T_{ox} . We have successfully determined this function, an analytical expression, that predicts the charge layer thickness with no more than V_g , V_t , and T_{ox} as inputs. This model has been verified against self-consistent solutions of the Schrodinger equation and Poisson equation for 15 different MOSFET technologies. A new version of BSIM3 with a CV model based on this research was released in December 1997.

MOSFET gate oxide scaling limits were investigated with respect to time-dependent breakdown, defects, plasma process damage, mobility degradation, poly-gate depletion, inversion layer thickness, tunneling leakage, charge trapping, and gate delay. It was projected that the operating field will stay around 5MV/cm for reliability and optimum speed. Tunneling leakage prevents scaling below 2nm, which is sufficient for MOSFET scaling to 0.05 μ m.

2. PRINCIPAL INVESTIGATORS

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Prof. Jeff Bokor

3. DEGREES AWARDED

Jeffrey Margolies, M.S. 1996
Edward Budiarto, Ph.D. 1997
S. Jeong, Ph.D. 1997 (Physics)
Farib Assaderaghi, Ph.D. 1995
Kai Chen, Ph.D. 1997

4. LISTING OF PUBLICATIONS

1. K. Chen, J. Duster, H. Wann, T. Tanaka, M. Yoshida, P.K. Ko, C. Hu, "Universal MOSFET Carrier Mobility Model and Its Application in Device Modeling and Optimization," Proc. 1995 Int'l Semiconductor Device Research Symposium, pp. 607-610, December 1995.
2. J. Son, S. Jeong, and J. Bokor, "Non Contact Probing of Metal-Oxide-Semiconductor Inversion Layers: Annealing Temperature Dependence of Mobility," Appl. Phys. Letters, pp. 1779-1780, September 1996.
3. E. Budiarto, J. Margolies, S. Jeong, J. Son, and J. Bokor, "High Intensity Thz Pulses at 1 kHz Repetition Rate," IEEE J. Quantum Electron, Vol. 32, pp. 1839-1846, October 1996.
4. C. Hu, "Gate Oxide Scaling Limits and Projection," Technical Digest of International Electron Devices Meeting, pp. 319-322, December 1996.
5. S. Jeong, S., Zacharias, H., Bokor, J., "Ultrafast Carrier Dynamics on the Si (100) 2*1 Surface," Physical Review B (Condensed Matter), Vol. 54, No. 24, pp. R17300-R17303, December 1996.
6. D. Sinitsky, R. Tu, C. Liang, M. Chan, J. Bokor, C. Hu, "AC Output Conductance of SOI MOSFETs and Impact on Analog Applications," IEEE Electron Device Letters, Vol., pp. 36-3818, February 1997.
7. F. Assaderaghi, D. Sinitsky, S. Park, J. Bokor, P. K. Ko, and C. Hu, "Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI," IEEE Trans. on Electron Devices, Vol. 44, No. 3, pp. 414-422, March 1997.
8. F. Assaderaghi, D. Sinitsky, J. Bokor, P. K. Ko, H. Gaw, and C. Hu, "High-Field Transport of Inversion-Layer Electrons and Holes Including Velocity Overshoot," IEEE Trans. on Electron Devices, pp. 664-671, April 1997.
9. D. Sinitsky, F. Assaderaghi, M. Orshansky, J. Bokor, and C. Hu, "An Extension of BSIM3 Model Incorporating Velocity Overshoot," Proc. of Int'l Symp. VLSI Tech., Systems and Applications, pp. 307-310, June 1997.
10. Y.-C. King, H. Fujioka, S. Kamohara, W.-C. Lee, and C. Hu, "AC Charge Centroid Model for Quantization of Inversion Layer in NMOSFET," Proc. of Int'l Symp. VLSI Tech., Systems and Applications, pp. 245-249, June 1997.
11. K. Chen, C. Hu, P. Fang, and A. Gupta, "Experimental Confirmation of an Accurate CMOS Gate Delay Model for Gate Oxide and Voltage Scaling," IEEE Electron Device Letters, pp. 275-277, June 1997.

12. E. Budiarto, N.-W. Pu, S. Jeong, and J. Bokor, "Near-Field Propagation of Terahertz Pulses from a Large Aperture Antenna," Opt. Lett., vol. 23, pp. 213-215, February 1998.

5. REPORTABLE INVENTIONS

None

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